A Monolithic X-band Class-E Power Amplifier

R. Tayrani

Raytheon Electronic Systems, 2000 East Imperial Highway El Segundo, CA 90245

Abstract:
This paper describes what is believed to be the first successful design and fabrication of a broadband monolithic high efficiency class-E driver amplifier that operates at X-band and employs a 0.3 um x 600 um pHEMT device. The amplifier's measured performance shows a peak Power Added Efficiency (PAE) of 63% at 10.6 GHz and a constant output power of greater than 24 dBm together with a gain of 10 dB over 9-11 GHz.

I. Introduction

Low cost, highly efficient, high power, microwave and RF amplifiers are required for many commercial, as well as defense system, applications. These include wireless LANs, wireless cable broadcast transmitters, cellular phones, and telecommunication systems, as well as advanced air-borne active phased array radar systems. The majority of these applications are very cost driven, and therefore the choice of technology, design methodology, and manufacturing cycle time are the major cost contributors and should be contained.

The aim of this paper is to provide a simple, yet accurate, design methodology for successful realization of switching mode, class-E high efficiency power amplifiers. Furthermore, a technique for modifying pHEMT large-signal model is described that yields a more accurate modeling of switching mode amplifiers. All aspects of circuit simulations, including time domain analysis, Harmonic Balance analysis, and large signal stability analysis were performed using Agilent ADS circuit simulator [1].

The first monolithic version of a class-E switching-mode amplifier operating at 835 MHz was reported in 1994 [2]. The class-E amplifier is essentially a tuned circuit, as shown in Figure 2, with current and voltage time-waveforms that are in anti-phase and therefore, theoretically dissipate zero power. The active device, in this case a pHEMT, acts as an ideal switch, driven to ON and OFF conditions by the input RF signal. The ideal AC load line for the pHEMT transistor is shown in Figure 1(b). It can be seen that the operating point moves along the Vds and Idss axes; i.e. the device is either OFF (in the saturated region) or ON (in the linear region). Therefore, the output voltage and current values at the device terminal do not exist simultaneously and the dissipated RF energy in the device is zero, leading to 100% theoretical amplifier efficiency.

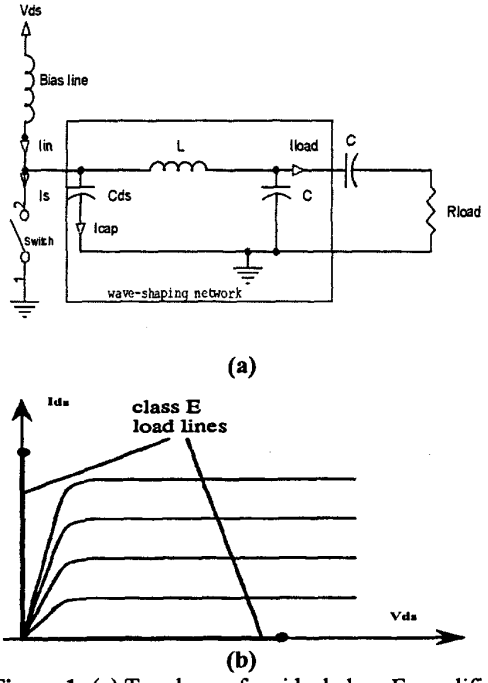

Figure 1: (a) Topology of an ideal class-E amplifier circuit. (b) Load line of a transistor in class-E regime.

With the advent of active device performance and monolithic circuit technology in the last five years, significant progress has been noted towards the development of high efficiency RF and microwave components. In the case of class-E high efficiency amplifiers, the circuit designers have pushed the useful operating frequency of these types of

amplifiers to ever-higher frequencies [3-4]. Looking further ahead, we envisage that by using innovative circuit topologies and device designs, it may be feasible to extend the useful operating frequency range of the switching mode amplifiers to Ku-band and possibly beyond.

II. Design Methodology and Circuits

A typical design procedure would follow the four main steps described below:

1. A simple ideal analytical design process that is based on a set of closed-form equations. The outcome of this step would yield the element values for the circuit topology shown in Figure 1(a).
2. A time domain analysis and optimization of the above topology to assure optimum voltage and current waveforms across the switch terminals as well as across Cds and the load terminals.
3. Development of a non-linear model for the pHEMT device and its modification for switching mode operation.
4. Harmonic Balance analysis of the complete circuit including large signal stability analysis.

Step 1:

The detailed analysis and derivation of the following expressions are fully discussed elsewhere [3], and therefore we will merely refer to them for the intended application. Knowing the device drain to source capacitance (C_{ds}) and the drain voltage (V_{ds}), an approximate maximum frequency (f_{max}) for class-E operation can be obtained. Similarly, assuming a load resistance of 50 ohms, one could obtain approximate values for the circuit elements of the wave-shaping network shown in Figure 1(a). These expressions are:

$$f_{\max} = \frac{I_{\max}}{56.5 C_{ds}},$$

$$L = \frac{0.28}{\omega^2 C_{ds}} \left[\sin\theta_0 + \cos\theta_0 \sqrt{\frac{\omega_s C_{ds} R}{k_0 \cos\theta} - 1} \right]$$

$$C = \frac{1}{\omega_s R} \sqrt{\frac{\omega_s C_{ds} R}{k_0 \cos\theta_0 - 1}}$$

Where: $k_0 = 0.28$, $\theta_0 = 49.05°$, $\omega = 2\pi f_{max}$

Step 2:

Having obtained the starting values for the load network, it is worthwhile to perform a time domain analysis on the circuit shown in Figure 1(a). The aim is to examine the current and voltage waveforms at appropriate terminals and optimize them for switching mode Class-E operation. It is also noteworthy to mention that in our time domain simulation and optimization, we have added a one-ohm internal resistance to the switch to obtain more realistic current and voltage waveforms. Figure 2 shows the simulation results for the circuit after optimization of the load network. The voltage waveform across the switch rises slowly at switch-off and falls to zero at the end of the half-cycle. It also has a zero rate of change at the end of half-cycle, thereby ensuring a "soft" turn-on condition.

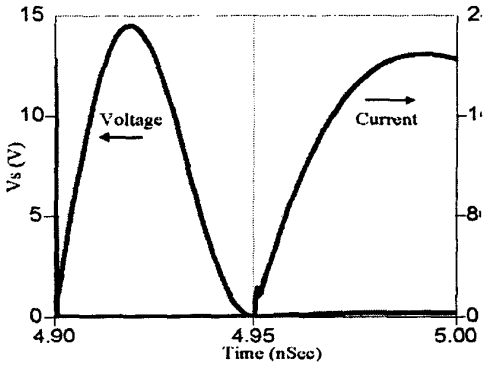

Figure 2: Switch voltage and current waveforms

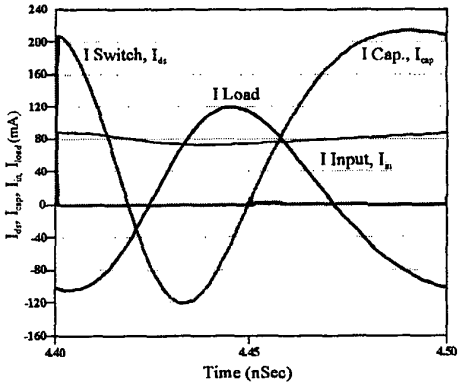

Figure 3: Current waveforms for circuit (1a)

The voltage across the switch when it is off is defined by the integral of the current flowing through C_{ds}. The phase shift introduced by the LC circuit adjusts the point at which the current is diverted from the

switch to the capacitor C_{ds}. Therefore, to ensure class-E operation, it is essential that the integral of capacitor current over the half-cycle is zero and that the capacitance current has dropped to zero by the end of the half-cycle. Figure 3 shows that the optimized current waveforms comply with the aforementioned criteria for class-E amplifiers.

Step 3:

The majority of the existing non-linear pHEMT models available in the commercial circuit simulators are not suitable for modeling class-E circuits. For accurate modeling of switching mode amplifiers, the model should have the following important properties:

- Bias dependency of drain-to-source $C_{ds}(V_{ds},V_{gs})$ and gate-to-drain C_{gd} (V_{ds},V_{gs}) capacitances
- Bias dependency of input channel resistance $R_i(V_{ds},V_{gs})$
- Bias dependency of output channel resistance $R_{ds}(V_{ds},V_{gs})$
- A two current generator dispersion model for accurate simulation of R_{ds}

The use of any non-linear models that model the dispersive behavior of the output resistance by a simple series resistor-capacitor network, connected in parallel to the standard output network, should be conducted with care. In such a case, the loading effect of the series resistor-capacitor network on the output resistance should be removed.

After careful observation of the available non-linear models, we decided on the EEHEMT model [1] as a suitable choice for the non-linear simulation of class-E amplifiers. The most distinguishing features of this model for class-E are the ability to model R_{ds}(Vds, Vgs) and its dispersion effect, as well as the bias dependencies of the device capacitances.

Step 4:

Having obtained the optimized load impedance from step two and the non-linear model coefficients from step 3, the next step is to design the final amplifier topology. At this stage, there are several design approaches that one may follow; therefore, the suggested process is not unique, but, in our experience, it has proven to be successful.

Our design objective was to develop a class-E monolithic amplifier operating over 9-11 GHz using a 0.3 um x 600 um pHEMT device. The design process starts by generating the large signal S-parameters of the device over the desired RF input drive and frequency band while the device stability is assured by conventional circuit techniques. The next stage is to design the input-matching network for the amplifier by providing a conjugate match to the large signal S11 over the frequency band of interest (9-11GHz, in this case). Figure 4 shows the final schematic circuit of the amplifier.

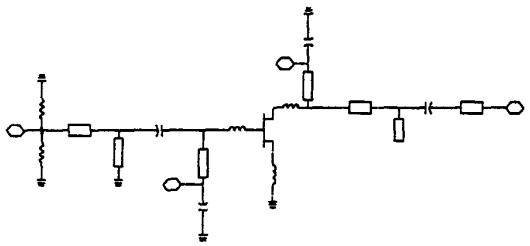

Figure 4: X-band Class-E amplifier

Figure 5 depicts the simulated voltage and current waveforms at the pHEMT output terminals of the amplifier. The waveforms confirm the switching mode behavior of the pHEMT, a condition that is necessary for class-E operation of the amplifier.

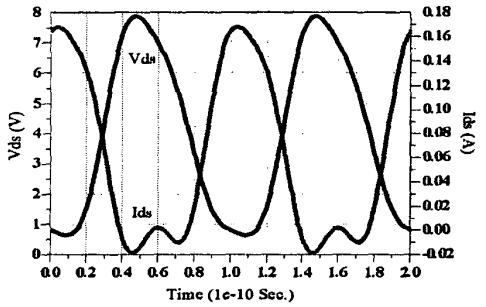

Figure 5: Simulated waveforms of the class-E amp.

III. Measured Performance

The completed monolithic amplifier chip is shown in Figure 6. A primitive layout was used in this first iteration to assure the accuracy of the complex load.

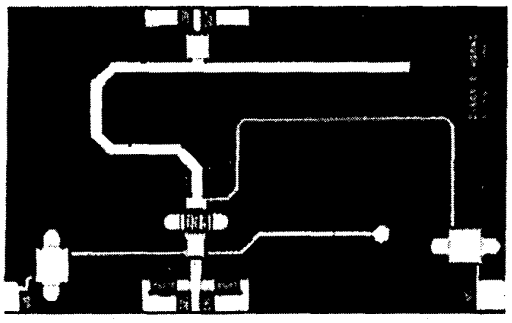

Figure 6: MMIC Amplifier chip (1.5mmx0.6mm)

Figure 7 shows the measured output power, PAE, and gain vs. input power at 10.6 GHz. A maximum efficiency of 63%, and an output power of 24 dBm is obtained at P_{in}=14 dBm. Figure 8 shows the measured amplifier output power for different values of RF input drive levels (0-18 dBm) over 7-12 GHz. As it can be seen, a broadband output power is obtained indicating the broadband capability of class-E operation. Figure 9 depicts the measured amplifier power added efficiency (PAE) for different RF input drive levels. PAE of greater than 40% over 9-11 GHz, peaking to 63% at around 10.6 GHz is obtained.

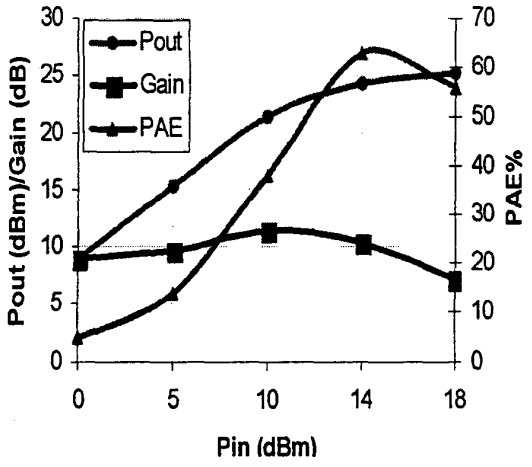

Figure 7: Measured output power, PAE, and gain vs. input power at 10.6 GHz.

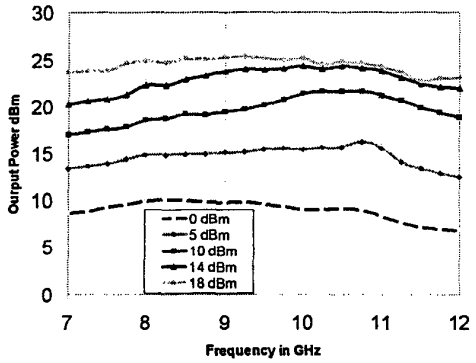

Figure 8: Measured output power, vs. frequency

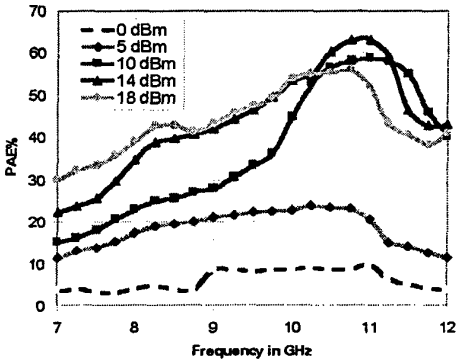

Figure 9: Measured PAE vs. frequency

IV. Conclusions

The first successful design and fabrication of an X-band monolithic high efficiency class-E amplifier has been reported. In addition, a four step design methodology is described. Based on this design approach, a monolithic amplifier that employs a 0.3 um x 600 um pHEMT device has been fabricated. The amplifier's measured performance shows a peak Power Added Efficiency (PAE) of 63% at 10.6 GHz and a constant output power of greater than 24 dBm together with a gain of 10 dB over 9-11 GHz.

References

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